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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,198	02/13/2004	Koji Arita	8001-1191	8942

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EXAMINER	
BERRY, RENEE R	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 10/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/777,198	ARITA ET AL.	
	Examiner	Art Unit	
	Renee R Berry	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) 1-12 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) 1-12 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,76,826 to Abe in view of US Patent No. 6,245,676 to Ueno.

In regards to claim 1, Abe teaches a method of manufacturing a semiconductor device comprising a process for forming a seed layer in a via hole or a wiring-trench formed in an interlayer insulating film formed on a semiconductor substrate, and then burying a wiring material using an electroplating method, wherein the current step of said plating method has only one step for flowing a current in the direction opposite to the direction for growing the plating at column 5, lines 54-64.

In regards to claim 12, Abe teaches the method of manufacturing a semiconductor device according to claim 1, wherein said wiring material is copper at column 5, lines 54-64.

However, Abe does not teach all the limitations of the claims.

In regards to claim 2, Ueno teaches the method of according to claim 1, manufacturing semiconductor device wherein said current step comprises three steps; a first step for flowing a current only in the direction for growing the plating; a second step

for flowing a current only in the direction opposite to the direction for growing the plating; and a third current step for flowing only in the direction identical to said first step; in the order of said first, second, and third steps at column 8, lines 18-25.

In regards to claim 3, Ueno teaches the method of manufacturing a semiconductor device according to claim 1, wherein said step flowing a current only the direction opposite to the direction for growing the plating is configured at column 8, lines 25-31

In regards to claim 4, Ueno teaches the method of manufacturing a semiconductor device according to claim 2, wherein said second current step is configured at column 9, lines 20-35

In regards to claim 5, Ueno teaches the method of manufacturing a semiconductor device according to claim 2, wherein said first current step is configured at column 9, lines 20-35.

In regards to claim 6, Ueno teaches the method of manufacturing a semiconductor device according to claim 4, wherein said first current step is configured so that the product of the current and the time is within a range between 120 and 2700 mA x sec/cm^2 10, lines 16-23 and lines 49-62

In regards to claim 7, Ueno teaches the method of manufacturing a semiconductor device according to claim 2, wherein the current value of said first current step is within a range between 0.5 and 13 mA/cm^2 at column 10, lines 16-23.

In regards to claim 8, Ueno teaches the method of manufacturing a semiconductor device according to claim 4, wherein the current value of said first current step is within a range between 0.5 and 13 mA/cm^2 at column 10, lines 16-23.

In regards to claim 9, Ueno teaches the method of manufacturing a semiconductor device according to claim 2, wherein the current value of said third current step is within a range between 16 and 90 mA/cm^2 at column 10, lines 16-23 and lines 49-62.

In regards to claim 10, teaches the method of manufacturing.a semiconductor device according to claim 4, wherein the current value of said third current step within a range between 16 and 90 mA/cm^2 10, lines 16-23 and lines 49-62.

In regards to claim 11, Ueno teaches the method of manufacturing a semiconductor device according to claim 6, wherein the current value of said third current step is within a range between 16 and 90 mA/cm^2 10, lines 16-23 and lines 49-62.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made, to have modified Abe to include manufacturing semiconductor device wherein said current step comprises three steps; a first step for flowing a current only in the direction for growing the plating; a second step for flowing a current only in the direction opposite to the direction for growing the plating; and a third current step for flowing only in the direction identical to said first step; in the order of said first, second, and third steps; and the current value of said first current step is

within a range between 0.5 and 13 mA/cm^2, since such a modification would result in a higher copper area ratio, as described in column 3, lines 54-57 of Ueno.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Renee R Berry whose telephone number is (571) 272-1774. The examiner can normally be reached on M-F 9-5:30.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RRB

September 17, 2004

GENE N. AUDUONG
PRIMARY EXAMINER